Programmer’s Guide to Yamaha YM3806 (OPQ) FM Synthesizer

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Summary

This document contains a programmer’s guide and a minimal data sheet for Yamaha OPQ FM synthesizer chips. The information applies to YM3806 and very propably to YM3533 also.

Disclaimer

Because most of the information presented here is based on reverse engineering, it is very probable that there are misunderstandings and omissions. The writer assumes no responsibility for any damages arising out of use of this text. No warranty is provided about correctness of any information in this file.

Table of Contents

1 Introduction

This document contains a programmer's guide and a minimal data sheet for Yamaha OPQ FM synthesizer chips. The information applies to YM3806 and very propably to YM3533 also.

There is no official information available for these chips. Everything presented in this document is based on three sources:

- Reverse engineering of Yamaha PSR-70 keyboard, by the author
    - https://retroandreverse.blogspot.com/search/label/PSR-70%20reverse%20engineering
- Yamaha PSR-70 Owner's Guide, by Yamaha Corporation 1985
    - http://www.synthmanuals.com/manuals/yamaha/psr-70/owners_manual/
- Yamaha PSR-70 Service Manual, by Yamaha Corporation 1985
    - https://elektrotanya.com/yamaha_psr-70_sm.pdf/download.html

One of the main information sources is the PSR-70 original internal software, which I have studied closely. I will be referring to it several times with the term ”PSR-70 firmware”.

As a comparison and reference, I have used the more widely known OPL2/OPL3, especially the excellent document ”Programmer's Guide to Yamaha YMF 262/OPL3 FM Music Synthesizer” by Vladimir Arnost. Testing things using Dexed soft synth (”closely modeled on the original DX-7 characteristics”) gave some insight. Also DX-11 seems to be very close to OPQ in many respects.

The OPQ is not that widely used, but it is found at least in PSR-60, PSR-70 and CLP-100 keyboards.

2 The OPQ synthesizer chip

The PSR-70 unit used for reverse engineering contains YM3806 chip, so all first-hand information here is from this chip. The Service Manual uses also name YM3533 interchangeably, so it should be the same chip.

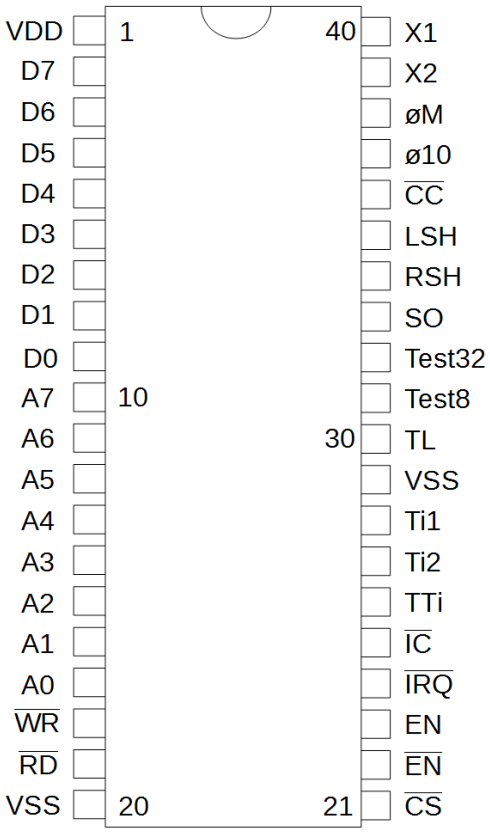
The chip is meant to be connected to normal processor bus. Data bus is 8-bit wide and there are 8 address lines. Bus control signals are the normal $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$. The chip can also request an interrupt.

OPQ chip contains no D/A-converter. It outputs two serial digital streams to an external DAC. In PSR-70, an YM3012 is used for this purpose. A datasheet for YM3012 is available in internet.

There is no bus timing information available. In PSR-70, a Z80 CPU with 6 MHz clock is used and the OPQ chip is mapped as a part of memory address space. There is a wait-

state logic implemented in hardware, but to my understanding it is not used when accessing the OPQ chip. This gives some rough idea about the bus timing specifications.

The chip comes in a 40-pin DIP package and the pinout is:



Pin functions:

VDD, VSS	5V supply
D7...D0	Data bus from/to CPU
A7...A0	Address bus from CPU
$\overline{WR}$, $\overline{RD}$	Write/read signals from CPU
$\overline{CS}$, $\overline{EN}$, EN	Chip select and enable signals from address decoding. In PSR-70 only $\overline{CS}$ is used, $\overline{EN}$ and EN are connected permanently active.
$\overline{IRQ}$	Interrupt request to CPU
$\overline{IC}$	Inital clear (= reset) from reset logic
SO, RSH, LSH	Serial data out to DAC. In YM3012, signals SD, SAM1, SAM2 respectively.
ø10	Clock out to DAC
X1, X2	Crystal. In PSR-70, a 3.579 MHz is used.

Pins not mentioned above are not connected anywhere in PSR-70, so it is impossible to say anything about their purpose.

3 OPQ synthesizer basics

Main specifications of the OPQ FM synthesizer:

- 8 voice channels, i.e. 8 voice polyphony
- 4 operators per channel, so there are 32 operators altogether
- 8 algorithms
- separate ADSR envelope generator for each operator
- one LFO, can be used for AM (tremolo) and FM (vibrato)
- monophonic (non-stereo) output

There is no percussion mode nor ”sacrifice channel count and get more operators per channel”-modes as in OPL3. This makes OPQ more straightforward from programmer's point of view.

The ”stereo or not stereo” question is quite clear: it is not stereo. The digital signals going to the DAC are named LSH and RSH, which gives a clue of Left and Right, but it is better to think that there are two separate output channels, and each voice channel can be sent to either of them or both. This can be useful for routing purposes but it is not stereo. The arrangement is similar to OPL3 synthesizer. Even PSR-70 does not use the output channels as left and right, it uses them for controlling the effects routing.

3.1 Operators and channels

Against Yamaha tradition, I will be numbering everything starting from 0, also the operators.

This table summarizes which operators form each channel's channel-specific operators:

	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
Op0	0	1	2	3	4	5	6	7
Op1	8	9	10	11	12	13	14	15
Op2	16	17	18	19	20	21	22	23
Op3	24	25	26	27	28	29	30	31

Table 1. Operators

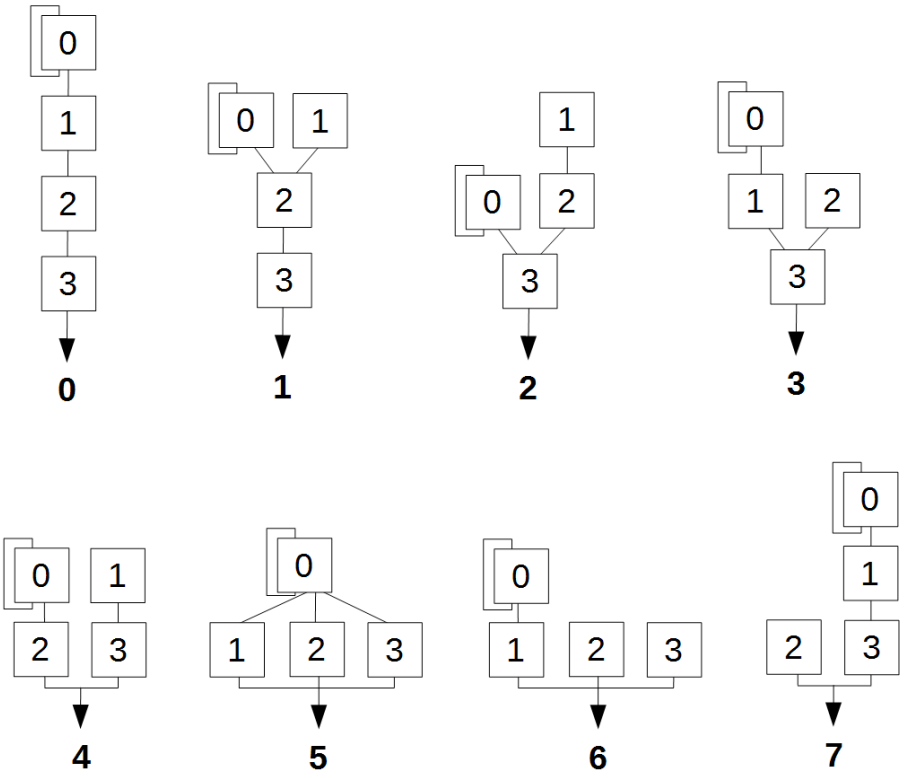
All four operators of one channel are not equal:

- In all algorithms, Op3 is always a carrier, never a modulator. It is also kind of ”master operator” regarding to triggering, see chapter 3.3.

- In all algorithms, Op0 is always a modulator, never a carrier. It is also the only operator which can use feedback. The feedback possibility is indicated with the feeback loop around Op0 in the algorithm picture on next page.

3.2 Algorithms

There are 8 algorithms to select from. The algorithms are presented in the following picture.



3.3 Triggering principles

The operator triggering scheme is quite different from OPL3. With triggering I mean turning operators on and off with their corresponding key-on bit. The main difference to OPL3 is that the triggering is not done per channel, it is done per operator. This means that even same channel's operators can be turned on or off at different times. Turning operator on starts its envelope's attack phase and turning it off starts the release phase. This gives quite a few new possibilities in sound design. I have not noticed that PSR-70 firmware would make use of this possibility.

There are some limitations, though. As mentioned, Op3 acts as a master operator: it must always be triggered on, otherwise channel's other operators won't trigger at all. Similarly, when Op3 is triggered off, all other operators will be triggered off at the same time. But while Op3 is on, you can freely trigger other three operators on and off, even several times, if you want.

Also during release phase Op3 affects on the other operators: if Op3's retrigger is disabled and it has long release time, it will not retrigger before its output level has decreased near zero. During that time any other same channel's operator won't retrigger either, even if its own release time has already ended.

3.4 Frequency settings

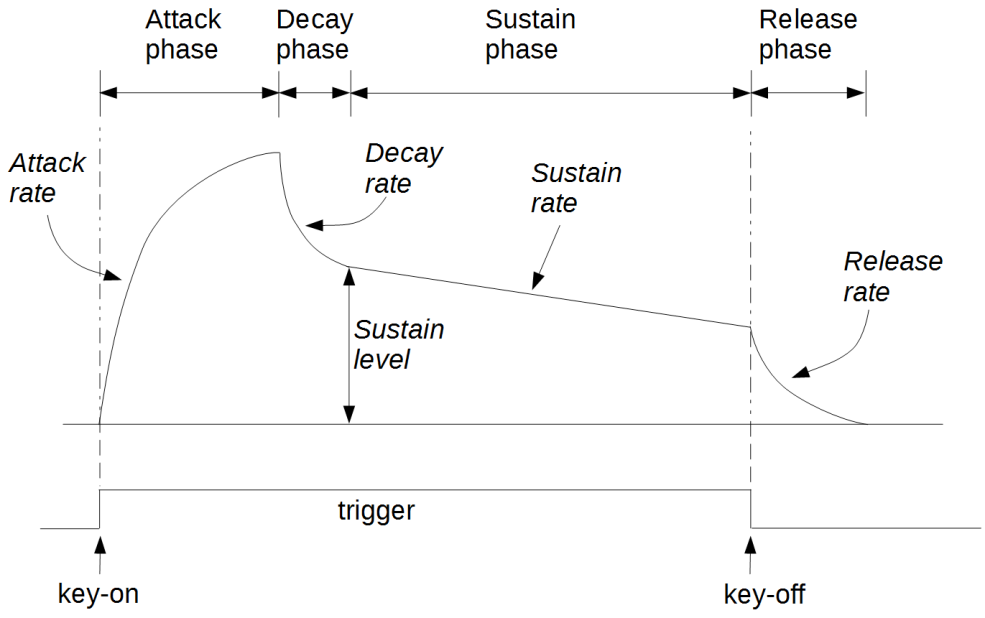
In OPQ each channel can have two different frequencies. Frequency is always set to an operator pair, meaning that two of the channel's operators can use one frequency, while two other can use completely different frequency. The two frequencies do not need to be in a harmonic relation, which again opens up interesting possibilities in sound design.

There is also possibility to detune each operator from its nominal frequency. And of course the frequency multiplication is available as always in FM.

3.5 Envelopes

Each operator has individually controllable envelope curve. In fact, half of the registers are used for the envelope settings.

OPQ envelope is a traditional ADSR-style envelope with one added parameter, sustain rate. During sustain phase the envelope curve can also decrease, and sustain rate controls the decrease rate. If sustain rate is 0, the sustain phase is horizontal (not decreasing), and the the envelope becomes basic ADSR. The curves are logarithmic in all phases, but with small values of sustain rate the curve is practically linear, as in the picture below.



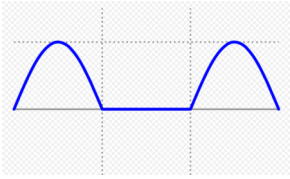
Attack, decay and release are given as rates. Rate defines how fast the curve changes. Larger rate = faster rise = shorter time. Also sustain rate is given as rate, but – as you might expect – it does not affect sustain time, it affects the final level at the key-off moment.

Sustain level defines the level, where the decay phase ends and sustain phase starts. So it affects to decay time also.

It looks like Yamaha DX-11 envelope system is exactly the same, just terminology differs. What I call here ”sustain” they call ”decay2”.

3.6 Waveforms

Each operator can have two different waveforms: sine and half-sine. Half-sine looks like this:



3.7 Timer and interrupts

OPQ chip contains one timer, which can generate repeating interrupts. In PSR-70 this is used as real-time interrupt with 10 ms interval. I did not find out, how this is actually controlled. I can get out 10 ms interrupts by mimicking the actions of the PSR-70 firmware, but that's all. I don't know how to alter the interval, for example.

Timer is the only thing inside OPQ which can cause interrupts. Sound generation does not use interrupts for anything.

The following chapters 4 and 5 are the actual register reference.

- Chapter 4 tries to answer questions like ”If I want to change attack rate of channel 4, operator 2, which register **address** should I write to?”
- Chapter 5 tries to answer questions like ”Now that I know the address, what is the **contents** of the data I should write to that register to change the attack rate?”

While describing registers, we will need hex numbers. For that purpose I will use the Intel/ Zilog originating style to use postfix 'H', like 0FH. If there is no 'H', the number is decimal.

4 Register structure

OPQ synthesizer has 256 8-bit registers, or at least 256 register addresses, not all have any functionality. All registers are write-only, except register 00H, which is read-only.

One big difference to OPL3 is that all registers are directly addressable, because the chip has 8 address lines. This makes writing and reading the registers simpler, no need for two-phase operations.

The registers show up as 256 consecutive addresses in the controlling processor's address space. This may be memory address space or I/O address space, depending on the hardware designer's decisions. In PSR-70, registers are in memory address space, because Z80 has only 256 register I/O address space, so the OPQ chip would alone eat up the whole I/O address space.

4.1 Register address groups

High level classification of registers can be done by grouping the registers in groups of 32 registers. The register group number is the 3 most significant bits in the register address.

Register group nr	Register adresses	Group's functionality
0	00H...1FH	General and channel specific settings
1	20H...3FH	Frequency settings
2	40H...5FH	Frequency multiplier/detune settings
3	60H...7FH	Output level settings
4	80H...9FH	Envelope: attack rate settings
5	A0H...BFH	Envelope: decay rate settings
6	C0H...DFH	Envelope: sustain rate settings
7	E0H...FFH	Envelope: sustain level/release rate settings

Table 2. Register groups

Register groups 0 and 1 need a bit more consideration, so lets look first at groups 2...7, which are more straightforward.

4.2 Register groups 2...7

In register groups 2...7 all settings are operator specific, meaning there is a register for each of the 32 operators and each operator may have different settings. The lower 5 bits of the register address can be thought as the operator number (0...31) and it can be mapped to channel number (0...7) and operator (Op0...Op3) using the table 1 on page 5.

But I like to think this in even simpler way. The setting can be written directly to specific channel's specific operator by dividing address bits like this:

A7	A6	A5	A4	A3	A2	A1	A0
RG2	RG1	RG0	ON1	ON0	CN2	CN1	CN0

RG2...RG0 (2...7): Register group number according to table 2.

ON1...ON0 (0...3): Channel's operator number, Op0...Op3.

CN2...CN0 (0...7): Channel number.

Examples:

- Attack rate setting of Ch5, Op0: address = 85H
- Sustain rate setting of Ch1, Op3: address = D9H

4.3 Register group 1

Register group 1 contains operator frequency settings. These settings are not operator specific, they are operator pair specific. The operator pairs are Op1+Op3 and Op0+Op2 for each channel, so there are 16 operator pairs altogether.

Although there are only 16 frequencies to be set, two for each channel, register group 1 still needs 32 registers. This is because each frequency is set by a 16-bit value, so there must be a high byte and a low byte for each operator pair.

The address is formatted like this:

A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	H	P	CN2	CN1	CN0

First three bits are 001, because this is register group 1.

H: Is this the high or low byte of the 16-bit frequency value?
0 = high byte
1 = low byte

P: Operator pair number
0 = Op1 + Op3
1 = Op0 + Op2

CN2...CN0: Channel number 0...7

Examples:

- Frequency of Ch5, Op0 and Op2: hi-byte address = 2DH, lo-byte address = 3DH
- Frequency of Ch1, Op1 and Op3: hi-byte address = 21H, lo-byte address = 31H

4.4 Register group 0

Register group 0 is the most heterogeneous one, it needs some subdivision.

- Addresses 00H...0FH contain couple of general (not channel or operator specific) settings and the status register. Most of the registers are not in use.
- Addresses 10H...1FH contain channel specific settings. They affect the channel as a whole, all operators at the same time. The 3 least significant bits of the address are the channel number.
    - 10H...17H = algorithm, feedback, output channel
    - 18H...1FH = vibrato, tremolo, echo control

5 Register contents

Each register is 8 bits wide. They are described here by register groups.

All registers are write-only, the value written cannot be read back. Only exception is register 00H, which is read-only.

Before writing to any register, software must check that BUSY-bit in register 00H is zero. At least this is how the PSR-70 firmware does it, I have not tested what happens, if you don't obey this.

5.1 Register addresses 00H...0FH

This register area contains only few registers that actually do something. Most registers seem not to affect anything.

5.1.1 Register 00H: Status register (read-only)

This is the only readable register. It returns status information. Following bits can be inferred from the PSR-70 firmware:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	-	-	-	-	INT1	-	INT2

BUSY — OPQ is busy. Every time PSR-70 firmware wants to write to any register, it first waits that this bit goes to 0.

INT1 — OPQ interrupt is active. This bit is 1 when OPQ has set its $\overline{\text{IRQ}}$-line active.

INT2 — Unknown. PSR-70 firmware tests for interrupt by masking register 00H value with 05H, so also this bit could be counted as an active interrupt. In my own tests I have never seen this bit active.

5.1.2 Register 03H: Timer control

This register controls the timer function. I have not figured out how the controlling is actually done, but every time the interrupt occurs, PSR-70 firmware writes 71H to this register. As a consequence, next interrupt occurs after 10 ms. I have copied this behavior to my own test programs and it works. If I don't write to this register, next interrupt will not occur.

This is not a counter start value or compare value, because it does not behave like that. It is possible to stop the interrupts coming by writing suitable values, but they don't make much sense. I have not found any way to control the interrupt interval.

5.1.3 Register 04H: LFO control

This controls the Low Frequency Oscillator. LFO can be used for tremolo and vibrato. LFO waveform is always triangle.

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	LDIS	LFO2	LFO1	LFO0

LDIS LFO enable/disable. 0 = LFO on, 1 = LFO off

LFO2...LFO0 LFO frequency, 0...7. Only values 0...6 are actually usable.

0 = about 4 Hz
...
6 = about 10 Hz
7 = about 47 Hz !

5.1.4 Register 05H: Key-on/key-off triggers

This register is the most heavily used register: it contains key-on/key-off triggers for all operators and all channels. This register is different from the basic principles in OPQ. Normally there is a register for each channel or each operator, but this one register handles them all.

D7	D6	D5	D4	D3	D2	D1	D0
-	KEY3	KEY2	KEY1	KEY0	CN2	CN1	CN0

KEY3 Key-on/off for this channel's Op3.

KEY2 Key-on/off for this channel's Op2.

KEY1 Key-on/off for this channel's Op1.

KEY0 Key-on/off for this channel's Op0.

CN2...CN0 Channel number 0...7

Writing a 1 to KEYn triggers envelope's attack phase. Writing a 0 triggers release phase. Only KEYn changes are relevant: writing same KEYn value as before does not trigger anything. Channel number defines, which channel's operators we are dealing with.

There are certain interdependencies and limitations between the operators; these are described in chapter 3.3.

5.2 Register addresses 10H...1FH

This register area contains channel specific settings. All settings affect the whole channel. Channel number is the 3 least siginficant bits of the register address.

5.2.1 Registers 10H...17H: Algorithm / feedback / output channel

D7	D6	D5	D4	D3	D2	D1	D0
OCH1	OCH2	FB2	FB1	FB0	ALG2	ALG1	ALG0

OCH1 — This channel's output is connected to output channel 1 (so called "right channel").

OCH2 — This channel's output is connected to output channel 2 (so called "left channel").

FB2...FB0 — Op0's feedback amount 0...7. 0 = no feedback, 7 = max feedback.

ALG2...ALG0 — Channel's algorithm 0...7. Algorithm numbering according to figure on page 6.

At least one of bits OCH1 or OCH2 must be set to hear the channel.

In PSR-70, output channel 1 is connected through chorus effect (not part of OPQ chip), channel 2 is connected directly.

5.2.2 Registers 18H...1FH: Vibrato / tremolo / echo

D7	D6	D5	D4	D3	D2	D1	D0
ECHO	VIB2	VIB1	VIB0	-	-	TR1	TR0

ECHO — This bit adds a short linear release ramp after operator's own release has ended. Sounds like a short echo when normal release is short. With long releases, you really cannot hear any effect.

VIB2...VIB0 — Amount of vibrato (frequency modulation by LFO), 0...7. 0 = no vibrato, 7 = max vibrato.

TR1...TR0 — Amount of tremolo (amplitude modulation by LFO), 0...3. 0 = no tremolo, 3 = max tremolo.

5.3 Register addresses 20H...3FH

Register group 1 contains operator frequency settings. All settings are operator pair specific. The addessing scheme is described in chapter 4.3.

5.3.1 Registers 20H...2FH: Octave / frequency hi-nibble

D7	D6	D5	D4	D3	D2	D1	D0
-	OCT2	OCT1	OCT0	FRQ11	FRQ10	FRQ9	FRQ8

OCT2...OCT0 Octave number 0...7.

FRQ11...FRQ8 4 most significant bits of the 12-bit frequency number.

5.3.2 Registers 30H...3FH: Frequency lo-byte

D7	D6	D5	D4	D3	D2	D1	D0
FRQ7	FRQ6	FRQ5	FRQ4	FRQ3	FRQ2	FRQ1	FRQ0

FRQ7...FRQ0 8 least significant bits of the 12-bit frequency number.

Octave and frequency number together define the operator's nominal frequency. The actual output frequency is still affected by detune and multiplier defined in registers 40H...5FH.

5.3.3 Octave and frequency numbering

Octaves are numbered so that the octave containing middle C (261.6 Hz) as the lowest note is octave number 4.

The 12-bit frequency number spans for one octave. Numbers used in PSR-70 firmware are:

Note	Freq number
C	4CAH
C#	513H
D	560H
D#	5B2H
E	609H
F	665H

Note	Freq number
F#	6C6H
G	72DH
G#	79AH
A	80EH
A#	889H
B	90AH

There is quite a large range of frequency numbers both under and above of the basic octave. According to my own measurements, the highest note which can be reached by changing only the frequency number, is the next octave's G#. At the low end the range is bigger: more than one octave below can be reached. This is good news while implementing pitch bend: no need to hassle with octave numbers during bend.

5.4 Register addresses 40H...5FH

Register group 2 contains frequency multiplier and detune settings. All settings are operator specific. The addressing scheme is described in chapter 4.2.

These registers serve dual purpose: the most significant bit defines the interpretation of the lower bits.

5.4.1 MSB = 0: Detune

D7	D6	D5	D4	D3	D2	D1	D0
0	-	DET5	DET4	DET3	DET2	DET1	DET0

DET5...DET0 Operator's detune amount 0...63.

Operator's frequency will be detuned from the nominal frequency set by registers 20H...3FH. Detune can be up or down. Detune amount 32 (20H) is the mid-point:

63 (3FH) = about 20 cents up
…
32 (20H) = no detune
…
0 (00H) = about 20 cents down

This means that you always have to write 20H to this register if you want the operator to be in tune!

5.4.2 MSB = 1: Frequency multiplier

D7	D6	D5	D4	D3	D2	D1	D0
1	-	-	-	MF3	MF2	MF1	MF0

MF3...MF0 Operator's frequency multiplication factor value 0...15. The actual frequency multiplier depends on the factor value according to the table below. The nominal frequency set by registers 20H...3FH will be multiplied by this.

Factor value	Multiplier
0	0.5
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	12
12	15
13	16
14	17
15	18

5.5 Register addresses 60H...7FH

Register group 3 contains operator output level settings. All settings are operator specific. The addressing scheme is described in chapter 4.2.

5.5.1 Output attenuation

D7	D6	D5	D4	D3	D2	D1	D0
-	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

ATT6...ATT0 Operator's output attenuation 0...127.
0 = no attenuation (max output level)
…
127 = max attenuation (operator silent)

Varying output level of a carrier varies the channel volume, and possibly timbre, if there are multiple carriers. Varying output level of a modulator varies the sound timbre.

5.6 Register addresses 80H...FFH

Rest of the register groups (4...7) contain envelope related settings. All settings are operator specific. The addressing scheme is described in chapter 4.2.

5.6.1 Registers 80H...9FH: Envelope: attack rate / key scaler

D7	D6	D5	D4	D3	D2	D1	D0
KSE2	KSE1	KSE0	AR4	AR3	AR2	AR1	AR0

KSE2...KSE0 Key scaler for envelope, 0...7. Scales all envelope times (attack, decay, release) by shortening times towards higher notes.
0 = light scaling (times are slightly shorter at higher notes)
…
7 = heavy scaling (times are much shorter at higher notes)

AR4...AR0 Attack rate 0...31.
0 = very slow (very long attack time)
…
31 = very fast (attack time about zero)

5.6.2 Registers A0H...BFH: Envelope: decay rate / waveform

D7	D6	D5	D4	D3	D2	D1	D0
TE/RD	WF	-	DR4	DR3	DR2	DR1	DR0

TE/RD — Tremolo (AM by LFO) enable. This bit defines whether the channel's tremolo is applied to this operator.
At the same time, this bit acts as a re-trigger disable. When this bit is set and operator has a long release time, it won't trigger again before release curve has decreased near zero.
Why these two completely separate settings are combined to this same bit, I cannot understand.

WF — Basic waveform of this operator.
0 = sine wave
1 = half-sine

DR4...DR0 — Decay rate 0...31.
0 = very slow (very long decay time)
…
31 = very fast (decay time about zero)

5.6.3 Registers C0H...DFH: Envelope: sustain rate

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	SR4	SR3	SR2	SR1	SR0

SR4...SR0 — Sustain rate 0...31.
0 = no decrease during sustain phase (sustain curve is horizontal, as in basic ADSR)
…
31 = very fast decrease during sustain phase

5.6.4 Registers E0H...FFH: Envelope: sustain level / release rate

D7	D6	D5	D4	D3	D2	D1	D0
SL3	SL2	SL1	SL0	RR3	RR2	RR1	RR0

SL3...SL0 Sustain level 0...15. This is the level where decay phase ends and sustain phase starts.

0 = max level

…

15 = zero level (no sound during sustain phase)

Setting sustain level = 0 also leads to the length of decay phase being 0.

RR3...RR0 Release rate 0...15.

0 = very slow (very long release time)

…

15 = very fast (release time about zero)

6 OPQ register table

Reg	Bit								Notes
	7	6	5	4	3	2	1	0	
General									
00H	BUSY	-				INT1	-	INT2	Read only
01H									Unused
02H									Unused
03H	?	?	?	?	?	?	?	?	Timer
04H	-				LDIS	LFO freq			LFO
05H	-	KEY3	KEY2	KEY1	KEY0	Channel nr			Triggers
06H...0FH									Unused
Algorithm / feedback / output – channel specific									
10H	OCH1	OCH2	Feedback			Algorithm			Channel 0
11H	OCH1	OCH2	Feedback			Algorithm			Channel 1
12H	OCH1	OCH2	Feedback			Algorithm			Channel 2
13H	OCH1	OCH2	Feedback			Algorithm			Channel 3
14H	OCH1	OCH2	Feedback			Algorithm			Channel 4
15H	OCH1	OCH2	Feedback			Algorithm			Channel 5
16H	OCH1	OCH2	Feedback			Algorithm			Channel 6
17H	OCH1	OCH2	Feedback			Algorithm			Channel 7
Vibrato / tremolo / echo – channel specific									
18H	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 0
19H	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 1
1AH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 2
1BH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 3
1CH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 4
1DH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 5
1EH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 6
1FH	Echo	Vibrato (FM)			-	-	Tremolo (AM)		Channel 7

Octave / frequency – operator pair specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
20H	-	Octave			Frequency Hi				Channel 0	Op1 & Op3
21H	-	Octave			Frequency Hi				Channel 1	
22H	-	Octave			Frequency Hi				Channel 2	
23H	-	Octave			Frequency Hi				Channel 3	
24H	-	Octave			Frequency Hi				Channel 4	
25H	-	Octave			Frequency Hi				Channel 5	
26H	-	Octave			Frequency Hi				Channel 6	
27H	-	Octave			Frequency Hi				Channel 7	
28H	-	Octave			Frequency Hi				Channel 0	Op0 & Op2
29H	-	Octave			Frequency Hi				Channel 1	
2AH	-	Octave			Frequency Hi				Channel 2	
2BH	-	Octave			Frequency Hi				Channel 3	
2CH	-	Octave			Frequency Hi				Channel 4	
2DH	-	Octave			Frequency Hi				Channel 5	
2EH	-	Octave			Frequency Hi				Channel 6	
2FH	-	Octave			Frequency Hi				Channel 7	
30H	Frequency Lo								Channel 0	Op1 & Op3
31H	Frequency Lo								Channel 1	
32H	Frequency Lo								Channel 2	
33H	Frequency Lo								Channel 3	
34H	Frequency Lo								Channel 4	
35H	Frequency Lo								Channel 5	
36H	Frequency Lo								Channel 6	
37H	Frequency Lo								Channel 7	
38H	Frequency Lo								Channel 0	Op0 & Op2
39H	Frequency Lo								Channel 1	
3AH	Frequency Lo								Channel 2	
3BH	Frequency Lo								Channel 3	
3CH	Frequency Lo								Channel 4	
3DH	Frequency Lo								Channel 5	
3EH	Frequency Lo								Channel 6	
3FH	Frequency Lo								Channel 7	

Frequency = 000H...FFFH (12 bits)
Octave = 0H...7H

Detune – operator specific

Same registers as multiplication factor, MSB = 0

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
40H	0	-	Detune						Channel 0	Op0
41H	0	-	Detune						Channel 1	
42H	0	-	Detune						Channel 2	
43H	0	-	Detune						Channel 3	
44H	0	-	Detune						Channel 4	
45H	0	-	Detune						Channel 5	
46H	0	-	Detune						Channel 6	
47H	0	-	Detune						Channel 7	
48H	0	-	Detune						Channel 0	Op1
49H	0	-	Detune						Channel 1	
4AH	0	-	Detune						Channel 2	
4BH	0	-	Detune						Channel 3	
4CH	0	-	Detune						Channel 4	
4DH	0	-	Detune						Channel 5	
4EH	0	-	Detune						Channel 6	
4FH	0	-	Detune						Channel 7	
50H	0	-	Detune						Channel 0	Op2
51H	0	-	Detune						Channel 1	
52H	0	-	Detune						Channel 2	
53H	0	-	Detune						Channel 3	
54H	0	-	Detune						Channel 4	
55H	0	-	Detune						Channel 5	
56H	0	-	Detune						Channel 6	
57H	0	-	Detune						Channel 7	
58H	0	-	Detune						Channel 0	Op3
59H	0	-	Detune						Channel 1	
5AH	0	-	Detune						Channel 2	
5BH	0	-	Detune						Channel 3	
5CH	0	-	Detune						Channel 4	
5DH	0	-	Detune						Channel 5	
5EH	0	-	Detune						Channel 6	
5FH	0	-	Detune						Channel 7	

Detune = 00H … 20H … 3FH
down … none … up

Multiplication factor – operator specific

Same registers as detune, MSB = 1

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
40H	1	-	-	-	Multiplication factor				Channel 0	Op0
41H	1	-	-	-	Multiplication factor				Channel 1	
42H	1	-	-	-	Multiplication factor				Channel 2	
43H	1	-	-	-	Multiplication factor				Channel 3	
44H	1	-	-	-	Multiplication factor				Channel 4	
45H	1	-	-	-	Multiplication factor				Channel 5	
46H	1	-	-	-	Multiplication factor				Channel 6	
47H	1	-	-	-	Multiplication factor				Channel 7	
48H	1	-	-	-	Multiplication factor				Channel 0	Op1
49H	1	-	-	-	Multiplication factor				Channel 1	
4AH	1	-	-	-	Multiplication factor				Channel 2	
4BH	1	-	-	-	Multiplication factor				Channel 3	
4CH	1	-	-	-	Multiplication factor				Channel 4	
4DH	1	-	-	-	Multiplication factor				Channel 5	
4EH	1	-	-	-	Multiplication factor				Channel 6	
4FH	1	-	-	-	Multiplication factor				Channel 7	
50H	1	-	-	-	Multiplication factor				Channel 0	Op2
51H	1	-	-	-	Multiplication factor				Channel 1	
52H	1	-	-	-	Multiplication factor				Channel 2	
53H	1	-	-	-	Multiplication factor				Channel 3	
54H	1	-	-	-	Multiplication factor				Channel 4	
55H	1	-	-	-	Multiplication factor				Channel 5	
56H	1	-	-	-	Multiplication factor				Channel 6	
57H	1	-	-	-	Multiplication factor				Channel 7	
58H	1	-	-	-	Multiplication factor				Channel 0	Op3
59H	1	-	-	-	Multiplication factor				Channel 1	
5AH	1	-	-	-	Multiplication factor				Channel 2	
5BH	1	-	-	-	Multiplication factor				Channel 3	
5CH	1	-	-	-	Multiplication factor				Channel 4	
5DH	1	-	-	-	Multiplication factor				Channel 5	
5EH	1	-	-	-	Multiplication factor				Channel 6	
5FH	1	-	-	-	Multiplication factor				Channel 7	

Output attenuation – operator specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
60H	-	Attenuation							Channel 0	Op0
61H	-	Attenuation							Channel 1	
62H	-	Attenuation							Channel 2	
63H	-	Attenuation							Channel 3	
64H	-	Attenuation							Channel 4	
65H	-	Attenuation							Channel 5	
66H	-	Attenuation							Channel 6	
67H	-	Attenuation							Channel 7	
68H	-	Attenuation							Channel 0	Op1
69H	-	Attenuation							Channel 1	
6AH	-	Attenuation							Channel 2	
6BH	-	Attenuation							Channel 3	
6CH	-	Attenuation							Channel 4	
6DH	-	Attenuation							Channel 5	
6EH	-	Attenuation							Channel 6	
6FH	-	Attenuation							Channel 7	
70H	-	Attenuation							Channel 0	Op2
71H	-	Attenuation							Channel 1	
72H	-	Attenuation							Channel 2	
73H	-	Attenuation							Channel 3	
74H	-	Attenuation							Channel 4	
75H	-	Attenuation							Channel 5	
76H	-	Attenuation							Channel 6	
77H	-	Attenuation							Channel 7	
78H	-	Attenuation							Channel 0	Op3
79H	-	Attenuation							Channel 1	
7AH	-	Attenuation							Channel 2	
7BH	-	Attenuation							Channel 3	
7CH	-	Attenuation							Channel 4	
7DH	-	Attenuation							Channel 5	
7EH	-	Attenuation							Channel 6	
7FH	-	Attenuation							Channel 7	

Attenuation = 00H … 3FH
Level max … min

Envelope: attack rate / key scaler – operator specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
80H	Key scaler			Attack rate					Channel 0	Op0
81H	Key scaler			Attack rate					Channel 1	
82H	Key scaler			Attack rate					Channel 2	
83H	Key scaler			Attack rate					Channel 3	
84H	Key scaler			Attack rate					Channel 4	
85H	Key scaler			Attack rate					Channel 5	
86H	Key scaler			Attack rate					Channel 6	
87H	Key scaler			Attack rate					Channel 7	
88H	Key scaler			Attack rate					Channel 0	Op1
89H	Key scaler			Attack rate					Channel 1	
8AH	Key scaler			Attack rate					Channel 2	
8BH	Key scaler			Attack rate					Channel 3	
8CH	Key scaler			Attack rate					Channel 4	
8DH	Key scaler			Attack rate					Channel 5	
8EH	Key scaler			Attack rate					Channel 6	
8FH	Key scaler			Attack rate					Channel 7	
90H	Key scaler			Attack rate					Channel 0	Op2
91H	Key scaler			Attack rate					Channel 1	
92H	Key scaler			Attack rate					Channel 2	
93H	Key scaler			Attack rate					Channel 3	
94H	Key scaler			Attack rate					Channel 4	
95H	Key scaler			Attack rate					Channel 5	
96H	Key scaler			Attack rate					Channel 6	
97H	Key scaler			Attack rate					Channel 7	
98H	Key scaler			Attack rate					Channel 0	Op3
99H	Key scaler			Attack rate					Channel 1	
9AH	Key scaler			Attack rate					Channel 2	
9BH	Key scaler			Attack rate					Channel 3	
9CH	Key scaler			Attack rate					Channel 4	
9DH	Key scaler			Attack rate					Channel 5	
9EH	Key scaler			Attack rate					Channel 6	
9FH	Key scaler			Attack rate					Channel 7	

Key scaler = 0H … 7H
Scaling light … heavy

Attack rate = 00H … 1FH
Attack time long … short

Envelope: decay rate / waveform / tremolo enable – operator specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
A0H	TE/RD	WF	-	Decay rate					Channel 0	Op0
A1H	TE/RD	WF	-	Decay rate					Channel 1	
A2H	TE/RD	WF	-	Decay rate					Channel 2	
A3H	TE/RD	WF	-	Decay rate					Channel 3	
A4H	TE/RD	WF	-	Decay rate					Channel 4	
A5H	TE/RD	WF	-	Decay rate					Channel 5	
A6H	TE/RD	WF	-	Decay rate					Channel 6	
A7H	TE/RD	WF	-	Decay rate					Channel 7	
A8H	TE/RD	WF	-	Decay rate					Channel 0	Op1
A9H	TE/RD	WF	-	Decay rate					Channel 1	
AAH	TE/RD	WF	-	Decay rate					Channel 2	
ABH	TE/RD	WF	-	Decay rate					Channel 3	
ACH	TE/RD	WF	-	Decay rate					Channel 4	
ADH	TE/RD	WF	-	Decay rate					Channel 5	
AEH	TE/RD	WF	-	Decay rate					Channel 6	
AFH	TE/RD	WF	-	Decay rate					Channel 7	
B0H	TE/RD	WF	-	Decay rate					Channel 0	Op2
B1H	TE/RD	WF	-	Decay rate					Channel 1	
B2H	TE/RD	WF	-	Decay rate					Channel 2	
B3H	TE/RD	WF	-	Decay rate					Channel 3	
B4H	TE/RD	WF	-	Decay rate					Channel 4	
B5H	TE/RD	WF	-	Decay rate					Channel 5	
B6H	TE/RD	WF	-	Decay rate					Channel 6	
B7H	TE/RD	WF	-	Decay rate					Channel 7	
B8H	TE/RD	WF	-	Decay rate					Channel 0	Op3
B9H	TE/RD	WF	-	Decay rate					Channel 1	
BAH	TE/RD	WF	-	Decay rate					Channel 2	
BBH	TE/RD	WF	-	Decay rate					Channel 3	
BCH	TE/RD	WF	-	Decay rate					Channel 4	
BDH	TE/RD	WF	-	Decay rate					Channel 5	
BEH	TE/RD	WF	-	Decay rate					Channel 6	
BFH	TE/RD	WF	-	Decay rate					Channel 7	

Decay rate = 00H … 1FH
Decay time long … short

Envelope: sustain rate – operator specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
C0H	-	-	-	Sustain rate					Channel 0	Op0
C1H	-	-	-	Sustain rate					Channel 1	
C2H	-	-	-	Sustain rate					Channel 2	
C3H	-	-	-	Sustain rate					Channel 3	
C4H	-	-	-	Sustain rate					Channel 4	
C5H	-	-	-	Sustain rate					Channel 5	
C6H	-	-	-	Sustain rate					Channel 6	
C7H	-	-	-	Sustain rate					Channel 7	
C8H	-	-	-	Sustain rate					Channel 0	Op1
C9H	-	-	-	Sustain rate					Channel 1	
CAH	-	-	-	Sustain rate					Channel 2	
CBH	-	-	-	Sustain rate					Channel 3	
CCH	-	-	-	Sustain rate					Channel 4	
CDH	-	-	-	Sustain rate					Channel 5	
CEH	-	-	-	Sustain rate					Channel 6	
CFH	-	-	-	Sustain rate					Channel 7	
D0H	-	-	-	Sustain rate					Channel 0	Op2
D1H	-	-	-	Sustain rate					Channel 1	
D2H	-	-	-	Sustain rate					Channel 2	
D3H	-	-	-	Sustain rate					Channel 3	
D4H	-	-	-	Sustain rate					Channel 4	
D5H	-	-	-	Sustain rate					Channel 5	
D6H	-	-	-	Sustain rate					Channel 6	
D7H	-	-	-	Sustain rate					Channel 7	
D8H	-	-	-	Sustain rate					Channel 0	Op3
D9H	-	-	-	Sustain rate					Channel 1	
DAH	-	-	-	Sustain rate					Channel 2	
DBH	-	-	-	Sustain rate					Channel 3	
DCH	-	-	-	Sustain rate					Channel 4	
DDH	-	-	-	Sustain rate					Channel 5	
DEH	-	-	-	Sustain rate					Channel 6	
DFH	-	-	-	Sustain rate					Channel 7	

Sustain rate = 00H … 1FH
Sustain time long … short

Envelope: sustain level / release rate – operator specific

Reg	Bit								Channel / Op	
	7	6	5	4	3	2	1	0		
E0H	Sustain level				Release rate				Channel 0	Op0
E1H	Sustain level				Release rate				Channel 1	
E2H	Sustain level				Release rate				Channel 2	
E3H	Sustain level				Release rate				Channel 3	
E4H	Sustain level				Release rate				Channel 4	
E5H	Sustain level				Release rate				Channel 5	
E6H	Sustain level				Release rate				Channel 6	
E7H	Sustain level				Release rate				Channel 7	
E8H	Sustain level				Release rate				Channel 0	Op1
E9H	Sustain level				Release rate				Channel 1	
EAH	Sustain level				Release rate				Channel 2	
EBH	Sustain level				Release rate				Channel 3	
ECH	Sustain level				Release rate				Channel 4	
EDH	Sustain level				Release rate				Channel 5	
EEH	Sustain level				Release rate				Channel 6	
EFH	Sustain level				Release rate				Channel 7	
F0H	Sustain level				Release rate				Channel 0	Op2
F1H	Sustain level				Release rate				Channel 1	
F2H	Sustain level				Release rate				Channel 2	
F3H	Sustain level				Release rate				Channel 3	
F4H	Sustain level				Release rate				Channel 4	
F5H	Sustain level				Release rate				Channel 5	
F6H	Sustain level				Release rate				Channel 6	
F7H	Sustain level				Release rate				Channel 7	
F8H	Sustain level				Release rate				Channel 0	Op3
F9H	Sustain level				Release rate				Channel 1	
FAH	Sustain level				Release rate				Channel 2	
FBH	Sustain level				Release rate				Channel 3	
FCH	Sustain level				Release rate				Channel 4	
FDH	Sustain level				Release rate				Channel 5	
FEH	Sustain level				Release rate				Channel 6	
FFH	Sustain level				Release rate				Channel 7	

Sustain level = 0H … FH
max … min

Release rate = 0H … FH
Release time long … short

Version history

V 1.0	Mar 18, 2020	First version
V 1.1	Feb 27, 2021	Additions: - Chapter 5.6.2: TR/RD-bit controls also tremolo - Chapter 6 added Corrections: - Chapter 4.3: H-bit values corrected - Chapter 5.3.1: typo FRQ9 → FRQ8